Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-3 (Canceled)

Claim 4 (Currently Amended): A transposition circuit ~~as defined in claim 1, wherein said~~ for generating data packets arranged as a transposed matrix and obtained from data packets in the form of an N x N matrix (where N is an integer of 2 or greater) by interchanging the rows and columns of the original matrix, wherein N input terminals and N output terminals are provided;

N packets of data are output in parallel for each matrix column from said output terminals when N packets of data are input in parallel for each matrix row to said input terminals;

the transposition circuit is provided with N memory units [[whose]] having storage areas to accommodate N data packets, N first selectors [[whose]] having output ports [[are]] individually connected to [[the]] input ports of [[these]] the memory units, N second selectors [[whose]] having output ports [[are]] individually connected to said output terminals, and a control unit;

said first and second selectors [[have]] having N ports, and any of [[these]] the

ports of said first and second selectors are [[is]] used as an input port in accordance with selection signals from said control unit;

the ports of said first selectors are connected to [[the]] corresponding ones of the input terminals;

the ports of said second selectors are connected to the output ports of corresponding ones of the ~~corresponding~~ memory units; and

said control unit specifies prescribed storage areas in said memory units and generates, together with said selection signals, address signals for reading data from said memory units and writing data to said memory units.